Nixie HV Switching PSU

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Nixie HV Switching PSU

It's been a while since this page was originally written - in that time, RoHS has come in and some parts I originally specified have been discontinued. I've now modified some of the components to use compatible parts which should be reasonably widely available. If you have any problems, please let me know.

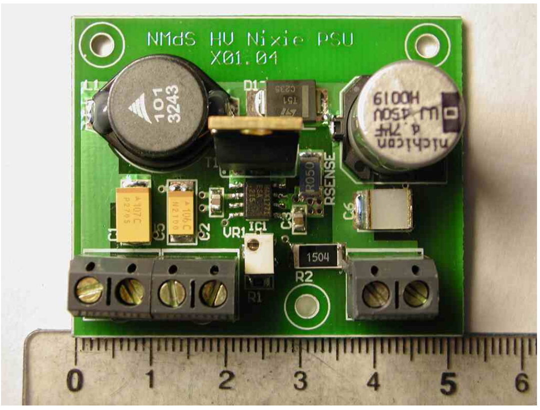
Note: The Eagle files accessed via the sidebar on this page have been updated to work with the latest versions of Eagle, including the MAC ones. There have also been some minor changes to the layout - however, some of the photos on this page have not yet been updated - this is of no consequence and does affect the relevance of any associated text.

Introduction

This particular project sprang from my fondness for nixies, a type of cold-cathode discharge display tube popular in the 1960's and 1970's, before they were effectively killed off by LEDs. There is a very active Google group called **NEONIXIE-L** which I can strongly recommend for those interested in these fascinating devices - see the left sidebar for more information

Nixies require a 170V to 250V DC power supply at between 10mA and 50mA - each tube actually only takes part of that, but certain types of tube take more than others, and, whatever people say, size matters - the bigger the tube, generally the more current it takes. Also, nixies tend to be used in multiples of two, normally these days for clocks. So, 4 tubes for a normal clock, 6 for something more elaborate... (hh:mm:ss etc.).

It was mentioned to me that this design could be appropriate for a number of low-current valve projects, as it happily provides a good, low-noise DC supply at high efficiency from a very small board with an input between 12V and 15V DC.



The core of this design is about 4cm x 3cm - using the main layout you can transport the PSU onto your own PCB with little effort,

Why a Switch-Mode Design?

It is probably beyond the scope of this simple document to describe the operation of switch-mode power supplies (SMPSs) - suffice to say the technique relies on the voltage pulse you get from rapidly collapsing the magnetic field in an inductor. This is done many thousands of times a second and the output pulses are collected and smoothed. Whilst this sounds simple, in practice it is complex to do well - there are a number of key design decisions that have to be made, and board layout is critical - SMPSs will not work well when built on Vero/StripBoard or prototyping plug-in boards - in fact, they may not work at all!

So, if SMPSs are tricky to work with, why use them? Simple - when they work they are brilliant! They are very small, cheap, completely solid-state, run cool and can be 90% or more efficient. This last point, efficiency, can be very important. SMPSs can lower a voltage (a "buck" converter) or increase the input voltage (a "boost" converter).

Suppose you wanted to drop a 9V supply to provide 5V @ 1A. If you used a linear voltage regulator, such as a 7805, you would be dropping 4V @ 1A in the regulator, i.e. dissipating 4W making it only 56% efficient (9W in, 5W out).

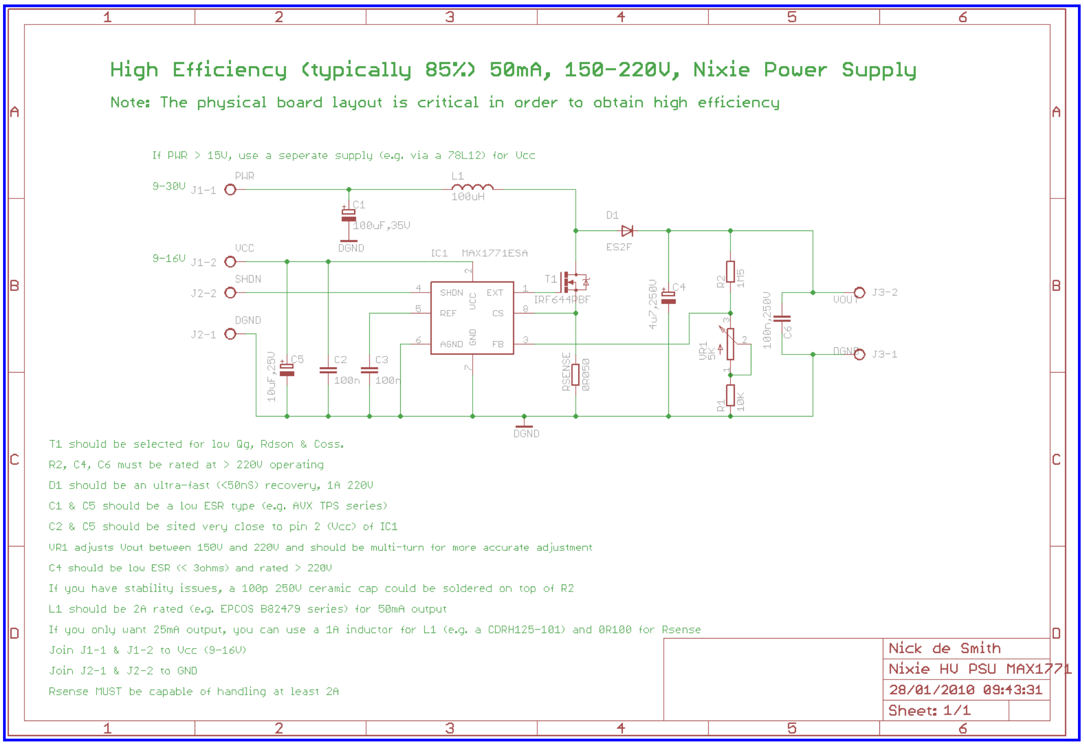
An SMPS buck converter doing the same job would typically be 90% efficient, so with a 5W output you would only have 5.6W in, i.e. about 0.6A in or only 2/3rds of the input current requirement of the linear regulator, not to mention only dissipating 0.6W - 6.7 times less than the linear "equivalent".

For boost converters, there is no easy linear equivalent - SMPSs are really the only choice unless you use a special transformer or an inverter, both of which are large - inverters tend to be complex and inefficient. The design given here will run at 88% efficiency when using the recommended layout and components. If you use another PCB layout, please, please read the notes about layout carefully - they really are important. The layout I use is the result of very careful experimentation and experience - you change the design, your results will be different - I guarantee it!

The Design

For this type of SMPS, there are a few chips that can be used. Manufactures include **MAXIM** (MAX771, MAX1771), **On Semiconductor** (MC34063) and others. My preferred chip is the MAX1771, a replacement for the deprecated MAX771. This chip uses a funky pulse-width modulation (PWM) scheme to get high efficiency in a variety of configurations, and has the added benefit of in-built current limiting.

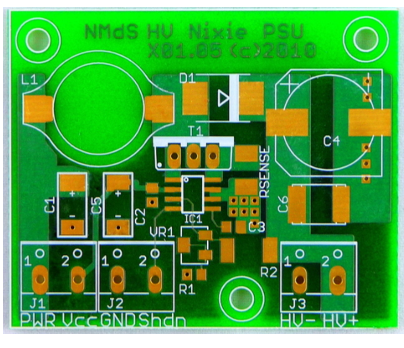
The circuit diagram may look similar to the examples in the **MAX1771 datasheet** - it is! However, for a configuration like this, where the step-up is large, what becomes absolutely critical is component choice and board layout.

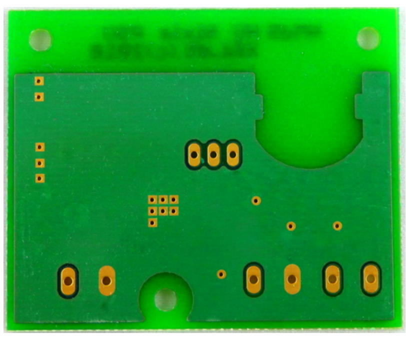


Click on the above schematic to see it full size and read the notes. The source for the project is all in **Eagle** and available from the link on the sidebar.

The key points are:

- Select the FET for low RDS_{on}, Q_g and C_{oss}. The FET I now use, a **Vishay IRF644PBF**, is a good choice as its not too exotic, is reasonably priced, and performs very well in this configuration with an RDS_{on} of 0R28 and Q_g of 69nC. An IRF740A (note the "A") will work but is more lossy.
- D1 needs to have a very fast M_{ttr}, typically < 50nS, but lower if possible. The device I chose, the **Vishay ES2F** has an M_{ttr} of 35nS.
- The trace between the MAX 1771 and the FET needs to be short and FAT, i.e. be low resistance and inductance. This allows the gate charge to be given to the FET in the shortest possible time; the speed the FET switches at directly effects efficiency.
- R2, the "top" end of the voltage feedback network, has almost the full output voltage across it. This point is often missed - most resistors are rated at 50V - run them at much above that for some time, and they will break down, so its important to use a 220V+ rated component.
- The FB pin is *very* sensitive to stray EMI - the voltage feedback network should be kept away from high current paths and the connection to the FB pin should be as short as possible. Should your implementation appear to not regulate or not to be adjustable, use a 'scope to have a look at the FB pin (3) - if you see spikes, then that may well be the reason. Putting a suppression capacitor from pin 3 to ground is *not* a solution - the layout must be correct.
- C1 & C5 should be low ESR types. This is important as they must provide high current very quickly - C1 provides up to a 2A surge into the inductor, and C5 the gate charge current for the FET.
- C2 & C5 should be close to the MAX 1771. This again is so that they can deliver the gate charge to the FET without interference from resistance or inductance in the PCB traces.
- C4, the output smoothing capacitor, must be low ESR, typically < 3 Ω. If a normal, high ESR capacitor is used then the regulator will have problems maintaining the output voltage under load. There are few choices available for high-voltage SMD aluminium electrolytics, but the Panasonic type V series EB are ok, e.g. EEV-EB2E100Q
- For 50mA+ output, L1 should be DC rated at about 2A. The chosen inductor, an EPCOS B82479, fits this bill and works very well in this circuit. If you use a shielded inductor, you will get less RFI, but the efficiency will also drop by about 3%. Small surface mount, high current, shielded inductors are not common! You could try a Sumida CDRH127-101 which works ok even though it starts to saturate at about 1.7A.
- For lower output currents up to 25mA, you can use a 1A inductor and change R_{sense} to 0R100 Ω. A good inductor here would be a Sumida CDRH125-101. Select an inductor with a low DC resistance as straight resistive losses will effect efficiency and lead to heating.
- It is sometimes a good idea to place an RF ferrite bead round the gate to the FET if you find that your circuit shows a tendency to be sensitive to the presence of a finger etc. e.g. when you move your hand near, you hear a whistle from the inductor or the output voltage varies.





My prototype PCBs were made by **Olimex** and show the implementation of the design rules above.

You can see the shadow of the **ground plane** on the underside and note that several vias in parallel have been used to connect R_{sense} to the **ground plane** - each via can typically handle a few 100 mA, and as up to 2A can flow through R_{sense} we need to provide a good low impedance path to ground. Note that there are no signal tracks on the bottom, thus the ground plane is un-interrupted.

Also, note the shortness of the gate trace to T1, the wide, low impedance main power traces and the lack of any loops that would lead to inductance losses. The tank capacitors are all close to the chip, as is the feedback adjustment. Stability is ensured by sensible layout.

The lack of a ground plane under the inductor prevents energy loss due to induced currents in the ground plane. If you look at the **top and**

bottom masks superimposed you will see that there is a clear area under the inductor and that we effectively have a "star" ground with no loops.

Performance Results

The performance results are available as a **PDF** file, but are repeated here. Testing was done using non-inductive high-power resistors. Rather than rely on the values printed, each was measured using a good DMM (Tektronix DMM 916). For each test, the input current and voltage was measured together with the output voltage. This gives us both the input and output power, and thus the efficiency.

Measurements were made after allowing each test setup to run for several minutes. At no time did any component get hot - the FET was always cool to the touch, and the inductor warmed up only under heavy loads, but never got hot.

MAX 1771 V4 Performance Tests

Experiment	V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	R_{load} (Ω)	I_{out} (mA)	P_{out} (W)	Efficiency (%)
1	12	0.33	3.96	181.75	9698	18.74	3.41	86.01
2	12	0.68	8.16	181.95	4685	38.84	7.07	86.60
3	12	0.92	11.04	175.52	3262	53.81	9.44	85.55
4	15	0.26	3.90	182.00	9698	18.77	3.42	87.58
5	15	0.54	8.03	182.10	4685	38.87	7.08	88.20
6	15	0.77	11.55	181.80	3262	55.73	10.13	87.72
7[1]	15	0.78	11.70	180.65	3262	55.38	10.00	85.51
8[2]	15.2	0.51	7.75	177.3	4685	37.84	6.70	86.60

[1]Experiment 7 used a shielded CDRH127-101 inductor rather than the default unshielded one. Note the efficiency drop vs. exp. 6

[2]Experiment 8 used a connection variation where the -ve end of C4 is connected to the CS input of the MAX1771 (pin 8, top end of the CS resistor, R_{sense}) rather than directly to ground. This mode of operation is discussed in the **Maxim Application Note, #1054, "Simple Change Improves PFM Boost-Controller Efficiency"**. As can be seen from these simple tests, in this rather extreme configuration, the change had no practicable effect on the efficiency of the circuit. Note that this test was not done on the original test PCB and there may well be subtle variations in the performance of individual boards. At best, when the original tests were repeated on the new board, an improvement of perhaps 0.25% could be seen, however this probably lies within the limits of experimental error and should be ignored.

- Ouput ripple was typically between 1% and 1.4%
- Switcher rate was approximately 62kHz
- If the default inductor (Epcos B82479-A1-104M) is replaced with a Sumida CDRH127-101 shielded inductor, then the overall efficiency drops by about 2% to 3%, but the level of radiated noise decreases. If RFI is a problem for you, this may be worth trying.

High Current Experiments

Some of the larger nixies, like the Rodan CD-47, require currents in the order of 25mA per tube. Experiments were carried out with using the same board layout as before, but using a higher current inductor, a higher current limit, and a FET that was selected for very low RDS_{on}. All other components remained as before, including the diode.

The choice of FET was important, as the original FET chosen (**IRFB9N30A**) has an RDS_{on} of 0R45Ω which can lead to losses of several Watts in a high current design when the FET spends a lot of its time on and conducting large currents. In the original low current design this was less of an issue as a trade-off was made between absolute performance and the cost of the FET. The new FET, **2SK3772-01** is far more expensive because of its extraordinarily good characteristics for a small TO220 package - normally, to get a low RDS_{on} you need a bigger die which means a bigger package (e.g. TO247) which in turn means a higher price - many of the true "exotic" FETs cost USD 15 or more

I have two other "exotic" FETs to try, both in TO247 cases: **APT30M85BVFR** (Farnell 382-9790) and **IXYS IXFH40N30** (Farnell 305-2576, DigiKey IXFH40N30-ND) - both have RDS_{on} values of 0R085Ω, but they are very expensive.

- R_{sense} changed to 0R025Ω (4A current limit)
- L1 changed to Newport Components 1400-series 47uH, 8.3A, 0R019Ω inductor. p/n 14.473.83 (Farnell p/n 482-572). The JW Miller 2200-series p/n 2209-H would probably be ok (DigiKey M9796-ND)
- T1 changed to Fuji Electric 2SK3772-01, RDS_{on} 0R130Ω, Q_g 44.5nC, V_{ds} 300V (Farnell p/n 120-8659)

MAX 1771 V4 Using 2SK3772-01 Performance Tests

Experiment	V_{in} (V)	I_{in} (A)	P_{in} (W)	V_{out} (V)	R_{load} (Ω)	I_{out} (mA)	P_{out} (W)	Efficiency (%)
1	14.92	1.85	27.60	187.45	1449	129	24.25	87.9
2	14.91	1.86	27.73	187.44	1449	129	24.25	87.4
3	14.91	1.67	24.90	177.83	1449	123	21.82	87.6

What can be seen from these results is that with a small change in component values allowing the use of a bigger inductor and a less lossy FET, we can make the SMPS produce 120+mA with no real problems.

I still have to try the other two (larger) FETS.

Bill of Materials

The following parts list has **Farnell** part numbers as I live in the UK, but most parts should be available from **DigiKey** or equivalent suppliers. The MAX 1771 is available as a sample from **MAXIM** if you are lucky!

Note that the DigiKey part numbers are not always the same component, but they represent a good compromise that is available from that supplier.

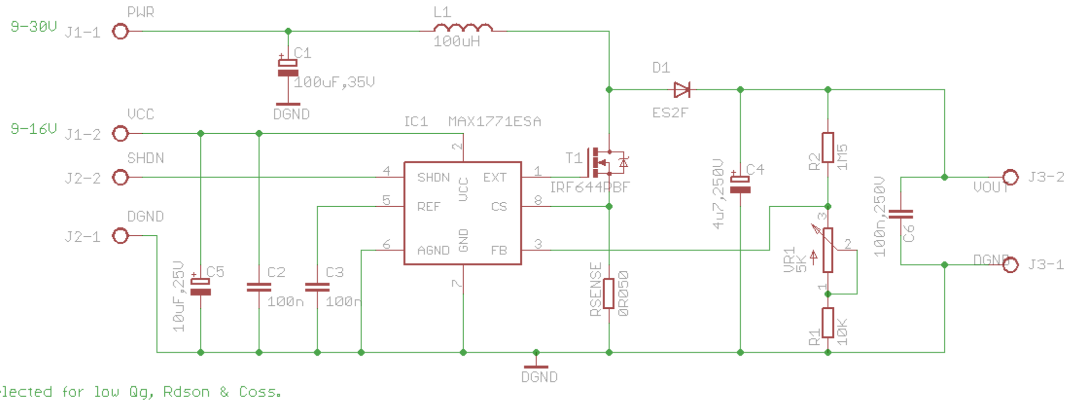
Part	Value	Package	Description	Manufacturer	Man. P/N	Farnell P/N	DigiKey P/N	Unit Cost (GBP qty. 1)	Comment
C1	100uF,35V	C-EIA-7343	Capacitor, Tantalum, EU 7343 case, polarised	AVX	TPSD107M035	570-412	478-1746-1-ND	1.31	Use lowest ESR available
C2,C3	100n	C0805	CAPACITOR, European symbol			n/a	490-1726-1-ND		Any generic 100nF 0805 cap
C4	10u7,250V	PANASONIC-ECG	Capacitor, Electrolytic, polarised	Panasonic	EEV-EB2E100Q		PCE3432CT-ND	0.68	Low ESR < 3ohms
C5	10uF,25V	C-EIA-7343	Capacitor, Tantalum, EU 7343 case, polarised	AVX	TPSW106M025	570-450	P11295CT-ND	0.62	Use lowest ESR available
C6	100n,250V	C2420		Panasonic	ECWU2104KC9	383-5625	PCF1412CT-ND	1.13	Optional
D1	ES2F	SMB	DIODE	ST	ES2F	162-5038	ES2F-E3/52TGITR-ND	0.74	Must have very fast mttr
IC1	MAX1771ESA	SO-8		Maxim	MAX1771ESA	n/a	MAX1771ESA-ND		Get from Maxim as a sample etc.
J1,J2,J3		SCREW-5MM-02	Twin 5mm-spaced connector block	IMO	20.100/2	RS:426-064	277-1236-ND	0.49	Any 5mm spacing connector (or just solder to the pads)
L1	100uH	L-B82479	SMT power inductors	Epcos	B82479-A1-104M	387-7693	436-1111-1-ND	3.31	2A or close
R1	10K	R0805	RESISTOR, European symbol			n/a	311-10.0KCCT-ND		Use any generic 10Kohm 0805 resistor
R2	1M5	R2512	RESISTOR, European symbol	Phicomp	PRC221 series	325-8142	PT1.5MXCT-ND	0.16	1 watt, 5%
RSENSE	0R050	R2010	RESISTOR, European symbol	Welwyn	LR2010-R05FW	110-0050	P50MCT-ND	0.66	2A current rating - 1Watt in a 2010 case
T1	IRF644PBF	TO220BV	N-CHANNEL MOS FET	Vishay	IRF644PBF	864-8409	IRF644PBF-ND	2.12	IRF740A will do (only "A" or "B" versions)
VR1	5K	BOURNS-3214W		Bourns	3214W-1-502E	988-261	3214W-502ECT-ND	1.58	Multi-turn - Any similar will do

Back

High Efficiency (typically 85%) 50mA, 150-220V, Nixie Power Supply

Note: The physical board layout is critical in order to obtain high efficiency

If PWR > 15V, use a seperate supply (e.g. via a 78L12) for Vcc



T1 should be selected for low Qg, Rdson & Coss.

R2, C4, C6 must be rated at > 220V operating

D1 should be an ultra-fast (<50nS) recovery, 1A 220V

C1 & C5 should be a low ESR type (e.g. AVX TPS series)

C2 & C5 should be sited very close to pin 2 (Vcc) of IC1

VR1 adjusts Vout between 150V and 220V and should be multi-turn for more accurate adjustment

C4 should be low ESR (< 3ohms) and rated > 220V

If you have stability issues, a 100p 250V ceramic cap could be soldered on top of R2

L1 should be 2A rated (e.g. EPCOS B82479 series) for 50mA output

If you only want 25mA output, you can use a 1A inductor for L1 (e.g. a CDRH125-101) and 0R100 for Rsense

Join J1-1 & J1-2 to Vcc (9-16V)

Join J2-1 & J2-2 to GND

Rsense MUST be capable of handling at least 2A

Nick de Smith
Nixie HV PSU MAX1771
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