

Estimating the voltage impressed on the tuning capacitor of a small transmitting loop

The 'net abounds with calculators for design of small transmitting loops (STL), and most estimate the voltage impressed on the tuning capacitor. Most of these calculators give an incorrect estimate.

This article describes a measurement based approach to estimating the capacitor voltage for a STL.

Theory

Most of the loss in a well implemented STL is in the main loop circuit, and that can be well approximated by a series equivalent circuit consisting of the loop's inductive reactance (X_L) in series with an equal capacitive reactance (X_C) and equivalent total series resistance R_s . The ratio $X_L/R_s = X_C/R_s = Q$.

Another representation is as a parallel equivalent circuit with the loop inductor, capacitor, and equivalent parallel resistance R_p all in parallel. The ratio $R_p/X_L = R_p/X_C = Q$.

The latter relationship gives a method for estimating voltage across X_C . Since $P = E_{rms}^2/R$, we can find the voltage across R_p by $E_{rms} = (P \cdot R_p)^{0.5}$ and substituting for R_p , $E_{rms} = (P \cdot Q \cdot X_L)^{0.5}$. Since $E_{pk} = 2^{0.5} \cdot E_{rms}$ for a sine wave, we can write $E_{pk} = (2 \cdot P \cdot Q \cdot X_L)^{0.5}$.

In practice

We will follow these steps:

1. X_L ;
2. find Q ; and
3. Calculate E_{pk} at given power.

Find X_L

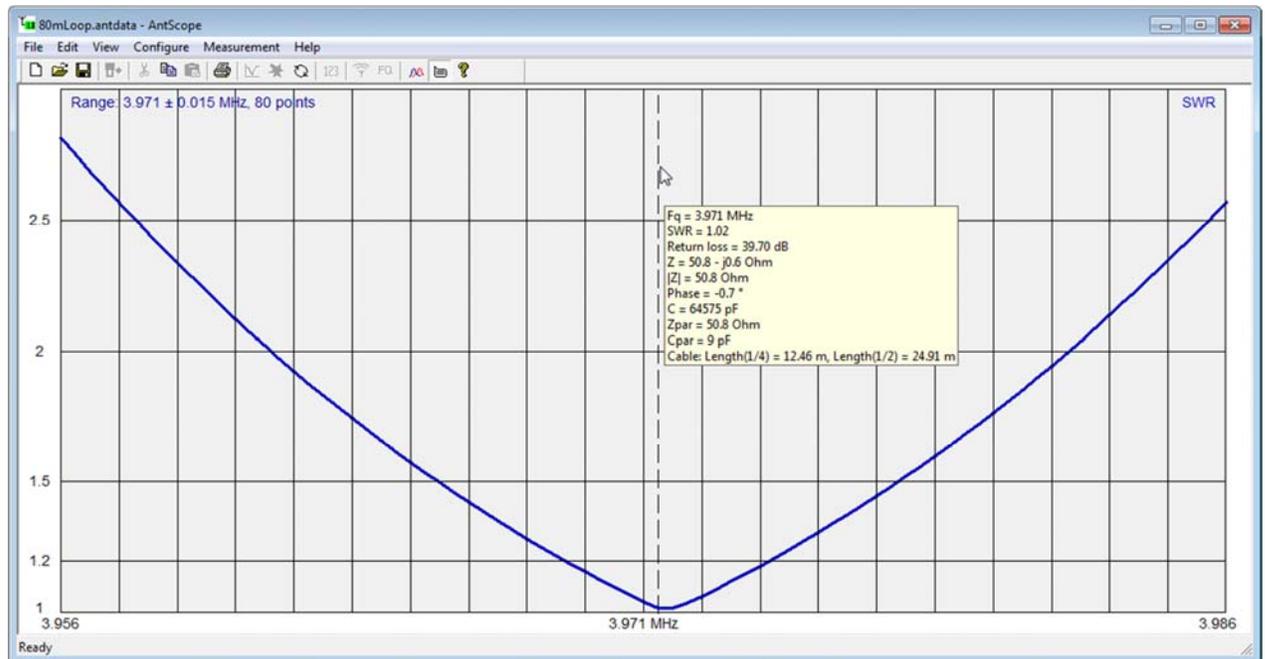
We can reliably calculate the inductance of a STL from a formula, or use direct measurement of the loop using a suitable antenna analyser or VNA. From that, $X_L = 2 \cdot \pi \cdot f \cdot L$.

For example, the inductance of a circular loop of 3.75m perimeter of 8mm diameter copper tube is $3.75 \mu H$, and at 4MHz $X_L = 94.3 \Omega$.

Find Q

Measure the half power bandwidth of the completed and matched antenna.

Here is an example measurement made of a STL using an AA-600 analyser



Above is the VSWR plot from the AA-600. VSWR=2.6 bandwidth corresponds to the half power bandwidth of the loop itself. Measured bandwidth is 30 kHz.

Calculate $Q = fc/BW = 4000/30 = 133.3$.

Calculate Epk at given power

Lets calculate Epk for 20W input power.

$$Epk = (2 * P * Q * XI)^{0.5} = (2 * 20 * 133.3 * 94.3)^{0.5} = 709Vpk.$$

This is the working voltage, you would choose a capacitor of somewhat higher rating.

You could use the actual capacitor breakdown rating less safety margin to find safe maximum power for the capacitor, so lets say you procured a 1800V capacitor and don't want to stress it beyond 1200V, rearranging the formula give earlier you can calculate $Pmax = Epk^2 / (2 * Q * XI) = 1200^2 / (2 * 133.3 * 94.3) = 57W$.

Reconciliation

We can learn from experiments that don't quite go to plan.

Does your loop implementation reconcile with the design tool you used?

Why?

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